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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--------------------------------------|-----------------------|-----------------------------|-------------------------|------------------|
| 10/662,734 | 09/15/2003 | Christopher Philip Ruemmler | 200311054-1 | 1494 |
| 22879 75 | 590 03/23/2006 | | EXAMINER | |
| HEWLETT PACKARD COMPANY | | | SONG, JASMINE | |
| P O BOX 2724 | 00, 3404 E. HARMONY I | ROAD | | |
| INTELLECTUAL PROPERTY ADMINISTRATION | | | ART UNIT | PAPER NUMBER |
| FORT COLLINS, CO 80527-2400 | | | 2188 | |
| | | , | DATE MAILED: 02/22/2004 | |

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| , | Application No. | Applicant(s) | | | | |
|--|--|-----------------------------|--|--|--|--|
| Ossia a Antina Carramana | 10/662,734 | RUEMMLER ET AL. | | | | |
| Office Action Summary | Examiner | Art Unit | | | | |
| | Jasmine Song | 2188 | | | | |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). | | | | | | |
| Status | | | | | | |
| 1) Responsive to communication(s) filed on 09 Ja | Responsive to communication(s) filed on 09 January 2006. | | | | | |
| , | | | | | | |
| <u></u> | | | | | | |
| closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. | | | | | | |
| Disposition of Claims | | | | | | |
| 4)⊠ Claim(s) <u>1-21</u> is/are pending in the application. | | | | | | |
| 4a) Of the above claim(s) is/are withdrawn from consideration. | | | | | | |
| 5) Claim(s) is/are allowed. | | | | | | |
| 6)⊠ Claim(s) <u>1-21</u> is/are rejected. | | | | | | |
| 7) Claim(s) is/are objected to. | | | | | | |
| 8) Claim(s) are subject to restriction and/or election requirement. | | | | | | |
| Application Papers | | | | | | |
| 9)☐ The specification is objected to by the Examiner. | | | | | | |
| 10)⊠ The drawing(s) filed on <u>09/15/2003</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner. | | | | | | |
| Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | |
| Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). | | | | | | |
| 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. | | | | | | |
| Priority under 35 U.S.C. § 119 | · | | | | | |
| 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: | | | | | | |
| 1. Certified copies of the priority documents have been received. | | | | | | |
| 2. Certified copies of the priority documents have been received in Application No | | | | | | |
| 3. Copies of the certified copies of the priority documents have been received in this National Stage | | | | | | |
| application from the International Bureau (PCT Rule 17.2(a)). | | | | | | |
| * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| | | | | | | |
| Attachment(s) | | | | | | |
| 1) Notice of References Cited (PTO-892) | 4) Interview Summary | • | | | | |
| 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | Paper No(s)/Mail Da 5) Notice of Informal Pa | atent Application (PTO-152) | | | | |
| Paper No(s)/Mail Date | 6) Other: | | | | | |

Detailed Action

1. This office action is in response to Amendment filed on 01/09/2006. Claims 1,10,11,19 and 21 have been amended. Claims 1-21 remain in the application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swanberg et al., US Patent 6,895,508 B1, in view of Draves et al., Us 5,950,221.

Regarding claim 1, Swanberg teaches that a memory system for a computer, the memory system comprising a single memory page (a single memory page is taught as a memory block 401 in the Fig.4A or a memory block in Fig.4B) including a kernel stack (it is taught as a program stack, a program stack is a block of memory defined with

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stack memory load and store instructions and a stack memory attribute identifying the stack memory as a program stack, col.4, lines 6-9 and the OS of the CPU associates a stack memory attribute in a page table with each block of memory accessed using a stack memory load/store instruction, col.4, lines 22-25; according to the Microsoft press computer Dictionary, Kernel is the core of an OS that manages memory, files, and peripheral devices; maintains the time and date; launches applications; and allocates system resources, therefore a program stack can be considered as the Kernel stack) and a register stack engine (RSE) stack (it is taught as a processor stack).

Swanberg does not specifically teach that the kernel stack is separate and distinct from user program stacks in the memory system.

However, Draves teaches that the kernel stack is separate and distinct from user program stacks in the memory system (col.5, lines 29-46).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Draves into Swanberg's stack memory system such as the kernel stack is separate and distinct from user program stacks in the memory system because it will prevent the user processes from interfering with kernel processes (col.3, lines 1-4 of Draves).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

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Regarding claim 11, Swanberg teaches that a compute system comprising:

a microprocessor including a register stack and a register stack engine (RSE) (a register stack is taught as a processor stack and the operating system is taught as a register stack engine; col.1, lines 45-46 and col.2, lines 11-13);

an operating system including a kernel (col.1, lines 14-16 and col.2, lines 11-13); and

a memory system configured to have a single memory page (a single memory page is taught as a memory block 401 in the Fig.4A or a memory block in Fig.4B) that includes both a kernel stack (it is taught as a program stack, a program stack is a block of memory defined with stack memory load and store instructions and a stack memory attribute identifying the stack memory as a program stack, col.4, lines 6-9 and the OS of the CPU associates a stack memory attribute in a page table with each block of memory accessed using a stack memory load/store instruction, col.4, lines 22-25; according to the Microsoft press computer Dictionary, Kernel is the core of an OS that manages memory, files, and peripheral devices; maintains the time and date; launches applications; and allocates system resources, therefore a program stack can be considered as the Kernel stack) and an RSE stack (it is taught as a processor stack).

Swanberg does not specifically teach that the kernel stack is separate and distinct from user program stacks in the memory system.

However, Draves teaches that the kernel stack is separate and distinct from user program stacks in the memory system (col.5, lines 29-46).

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It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Draves into Swanberg's stack memory system such as the kernel stack is separate and distinct from user program stacks in the memory system because it will prevent the user processes from interfering with kernel processes (col.3, lines 1-4 of Draves).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 21, Swanberg teaches that a method of a process entering a kernel of an operating system configured for an IPF processor architecture, the method comprising:

accessing a kernel stack (it is taught as a program stack, a program stack is a block of memory defined with stack memory load and store instructions and a stack memory attribute identifying the stack memory as a program stack, col.4, lines 6-9 and the OS of the CPU associates a stack memory attribute in a page table with each block of memory accessed using a stack memory load/store instruction, col.4, lines 22-25; according to the Microsoft press computer Dictionary, Kernel is the core of an OS that manages memory, files, and peripheral devices; maintains the time and date; launches applications; and allocates system resources, therefore a program stack can be

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considered as the Kernel stack) within a memory page (a single memory page is taught as a memory block 401 in the Fig.4A or a memory block in Fig.4B);

accessing an RSE stack (it is taught as a processor stack) within the same memory page (Fig.4A or Fig.4B); and

accessing a uarea data structure (it is taught as normal memory blocks such as memory block 505, col.4, lines 10-13) within the same memory page (Fig.5).

Swanberg does not specifically teach that the kernel stack is separate and distinct from user program stacks in the memory system.

However, Draves teaches that the kernel stack is separate and distinct from user program stacks in the memory system (col.5, lines 29-46).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Draves into Swanberg's stack memory system such as the kernel stack is separate and distinct from user program stacks in the memory system because it will prevent the user processes from interfering with kernel processes (col.3, lines 1-4 of Draves).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 2 and 12, Swanberg teaches that the kernel stack and the RSE stack grow in opposite directions (Fig.4B, col.3, lies 37-38).

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Regarding claims 3 and 13, Swanberg teaches that the single memory page further includes a "uarea" data structure (it is taught as normal memory blocks such as block 505, col.4, lines 10-13).

Regarding claims 4 and 14, Swanberg teaches that the uarea data structure is located between the kernel stack and the RSE stack (Fig.4B and Fig.5).

Regarding claims 5 and 15, Swanberg further teaches that a first red zone in a second memory page bordering a first memory region of the single memory page which is allocated to the kernel stack (it is taught as protected page or red zone 408).

Regarding claims 6 and 16, Swanberg further teaches that a second red zone in a third memory page bordering a second memory region of the single memory page which is allocated to the RSE stack (it is taught as protected page or red zone 409).

Regarding claims 7 and 17, Swanberg teaches that a number of translation lookaside buffer (TLB) misses when a process "enters" a kernel of an operating system of the computer is no more than one TLB miss (it is taught as the number of TLB miss will reduce when a memory address requested is associated with the memory stack attribute, col.3, lines 53 to col.4, lines 2).

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Regarding claims 9 and 20, Swanberg teaches that the memory system is used in cooperation with an operation system for the computer (col.3, lines 16-17), and wherein the operating system comprises a flavor of UNIX (Unix operating system is well know in the art).

Regarding claims 10 and 19, Swanberg teaches that the memory system is used in cooperation with at least one microprocessor with an IPF processor architecture (col.1, 29, IPF processor is taught as Intel IA 64).

Regarding claims 8 and 18, Swanberg teaches the claimed invention as shown above (claim 1 and 11), Swanberg does not teach that the memory system further comprises a stack overflow handler that is configured to allocate more memory to one of the stacks if it overflows. However, Draves teaches that the memory system further comprises a stack overflow handler that is configured to allocate more memory to one of the stacks if it overflows (col.5, lines 57-64). It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Draves into Swanberg's stack memory system such as employing a stack overflow handler that is configured to allocate more memory to one of the stacks if it overflows because it will preventing allocate-on-demand faults form occurring during execution of the stack overflow handler (col.3, lines 36-54).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated

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one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Response to Applicant's Arguments

5. Applicant's arguments with respect to claims 1-21 filed on 01/09/2006 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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7. When responding to the office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

8. When responding to the office action, Applicants are advised to provide the

examiner with the line numbers and page numbers in the application and/or references

cited to assist examiner to locate the appropriate paragraphs.

9. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jasmine Song whose telephone number is 571-272-

4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone

numbers for the organization where this application or proceeding is assigned are 571-

273-8300.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

3900.

Jasmine Song

Mano Padmanabhan 7/16/06

Patent Examiner

Supervisory Patent Examiner

March 15, 2006

Technology Center 2100

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINED

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